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PTO/SB/08A (10-01)  
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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
		Application / Conf. No.	09/991,410 / 3711
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Filing Date	November 16, 2001
		First Named Inventor	Nigel G. Herron
		Art Unit	2819
		Examiner Name	Unknown
		Attorney Docket Number	X-915 US
Sheet	1	of	1

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.¹	Document Number Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
27		US- 5,361,373	11-01-94	Gilson	
		US- 5,537,601	07-16-96	Kimura et al.	
		US- 5,652,904	07-29-97	Trimberger	
		US- 5,752,035	05-12-98	Trimberger	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Cite No.¹	Foreign Patent Document Country Code ² - Number ³ - Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁵

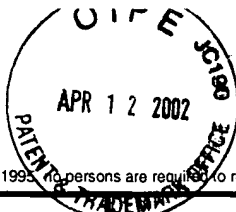
Examiner Signature	<i>D. Herron</i>	Date Considered	8/6/04
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Sheet 1 of 2

## Complete if Known

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First Named Inventor	Nigel G. Herron
Art Unit	2819
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Attorney Docket Number	X-915 US

## U.S. PATENT DOCUMENTS

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		Number - Kind Code (if known)			
DT		US- 5,671,355	09-23-97	Collins	
		US- 5,970,254	10-19-99	Cooke et al.	
		US- 6,020,755	02-01-00	Andrews et al.	
		US- 6,096,091	08-01-00	Hartmann	
		US- 6,279,045 B1	08-21-01	Muthujumaraswathy et al.	
		US- 6,282,627 B1	08-28-01	Wong et al.	
		US- 6,343,207 B1	01-29-02	Hessel et al.	
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## FOREIGN PATENT DOCUMENTS

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		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

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Signature

*Daniel J. ...*

Date  
Considered

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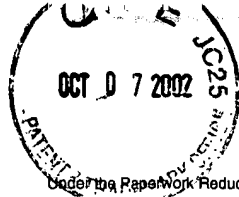
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Sheet

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		Number - Kind Code (if known)			
DT		US- 4,855,669	08-08-89	Mahoney	
		US-			
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## **FOREIGN PATENT DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>2</sup> - Number <sup>3</sup> - Kind Code <sup>4</sup> (if known)				

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Signature

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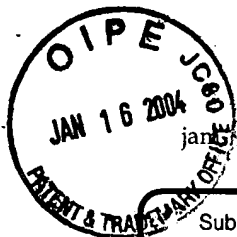
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Sheet 1 of 7

### Complete if Known

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Art Unit	2819
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Attorney Docket Number	X-915 US

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		Number - Kind Code (if known)				
DT		US- 4,758,985		07-19-88	Carter	
		US- 5,142,625		08-25-92	Nakai	
		US- 6,467,009		10-15-02	Winegarden et al.	
		US- 34,363		08-31-93	Freeman	
		US- 5,072,418		12-10-91	Boutaud et al.	
		US- 5,274,570		12-28-93	Izumi et al.	
		US- 5,550,782		08-27-96	Cliff et al.	
		US- 5,347,181		09-13-94	Ashby et al.	
		US- 5,339,262		08-16-94	Rostoker et al.	
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		US- 09/991,412		11-16-01	Herron et al.	
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		US- 5,740,404		04-14-98	Baji	
		US- 5,581,745		12-03-96	Muraoka	
		US- 5,742,179		04-21-98	Sasaki	
		US- 5,600,845		02-04-97	Gilson	
		US- 5,574,930		11-12-96	Halverson Jr., et al.	

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		Country Code <sup>2</sup> - Number <sup>3</sup>	Kind Code <sup>4</sup> (if known)				
DT		EP 0315275 A2		10-05-89	LSI Logic		
DT		WO 93 25968 A1		12-23-93	Furtek		
DT		EP 0 905 906 A2		03-31-99	Lucent		
DT		EP 1 235 351 A1		08-28-02	Matsushita Electric		

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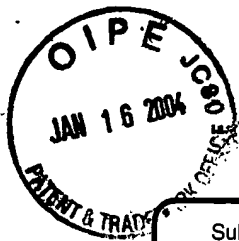
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application / Conf. No.	09/991,410 / 3711		
		Filing Date	November 12, 2000		
		First Named Inventor	Nigel G. Herron		
		Art Unit	2819		
		Examiner Name	Unknown		
Sheet	2	of	7	Attorney Docket Number	X-915 US

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OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
DT		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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DT		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	<i>David Tan</i>	Date Considered	8/6/04
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Sheet	3	of	7
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		Number - Kind Code (if known)			
DT ↓ ✓ DY		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 09/968,446	09-28-01	Douglass et al.	RECEIVED  JAN 22 2004  Technology Center 2100
		US- 6,026,481	02-15-00	New et al.	
		US- 5,705,938	01-06-98	Kean	
		US- 5,500,943	03-19-96	Ho et al.	
		US- 2003/0062922	04-03-03	Douglass et al.	
		US- 5,809,517	09-15-98	Shimura	
		US- 5,543,640	08-06-96	Sutherland et al.	
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		US- 6,604,228	08-05-03	Patel et al.	
		US- 5,933,023	08-03-99	Young	
		US- 6,510,548	01-21-03	Squires	
		US- 6,389,558	05-14-02	Herrmann et al.	
		US- 5,732,250	03-24-98	Bates et al.	
		US- 5,889,788	03-30-99	Pressly et al.	
		US- 5,874,834	02-23-99	New	
		US- 5,835,405	11-10-98	Tsui et al.	

## FOREIGN PATENT DOCUMENTS

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(use as many sheets as necessary)		Art Unit	2819		
		Examiner Name	Unknown		
Sheet	4	of	7	Attorney Docket Number	X-915 US

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OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
DT		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rte 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC," April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
DT		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

Examiner Signature	<i>Davidson</i>	Date Considered	8/6/04
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Substitute for form 1449A/PTO

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	5	of	7
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**Complete if Known**

<b>Application / Conf. No.</b>	09/991,410 / 3711
<b>Filing Date</b>	November 16, 2001
<b>First Named Inventor</b>	Nigel G. Herron
<b>Art Unit</b>	2819
<b>Examiner Name</b>	Unknown
<b>Attorney Docket Number</b>	X-915 US

## U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)	MM-DD-YYYY		
DT		US- 6,011,407	01-04-00	New	RECEIVED JAN 22 2004 Technology Center 2100
		US- 6,172,990	01-09-01	Deb et al.	
		US- 09/917,304	07-27-01	Douglass et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
		US- 5,892,961	04-06-99	Trimberger	
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		US- 09/861,112	05-18-01	Dao et al.	
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## FOREIGN PATENT DOCUMENTS

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Approved for use through 10/31/2002. OMB 0651-0031

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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<b>Application / Conf. No.</b>	09/991,410 / 3711
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<b>Art Unit</b>	2819
<b>Examiner Name</b>	Unknown
<b>Attorney Docket Number</b>	X-915 US

(use as many sheets as necessary)

Sheet	6	of	7	Attorney Docket Number	X-915 US
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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